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10/561,795	12/21/2005	Kiyoshi Kamiya	XA-10493	5851

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EXAMINER	
LO, KENNETH M	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
11/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/561,795	KAMIYA ET AL.	
	Examiner	Art Unit	
	Kenneth M. Lo	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/21/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 11/242149 has a total of 11 claims pending in the application; all of which are ready for examination by the examiner.

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

Drawings

2. The applicant's drawings submitted are acceptable for examination purposes.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of **50 to 150 words**. It is important that the abstract **not exceed 150 words** in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because Abstract exceeds proper length. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 11 is objected to because of the following informalities: Claim recites "wherein the control circuit can executes are write process". This sentence structure appears incorrect. Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1- 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the pieces of number-of-rewrites information" in line 13-14 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear which "pieces" are being referenced.

Claim 7 recites the limitation "the logical address" in Line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to which logical address this references.

Claim 9 recites the limitation "the number-of-rewrites information" in line 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitation "the number-of-rewrites information" in line 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "the pieces of number-of-rewrites information" in line 14-15 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear which "pieces" are being referenced.

Claim 12 recites the limitation "the pieces of number-of-rewrites information" in line 11-12 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear which "pieces" are being referenced.

Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph because they disclose a 'controller' which performs recited functions, however the controller is not claimed to contain any structural elements. It is unclear to the Examiner what structural elements are contained in the controller to perform the functions recited.

Claims 2-6, 8 are rejected based on their dependence on an earlier rejected claim.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-17** are rejected under 35 U.S.C. 102(b) as being unpatentable over Kaneda et al. [hereinafter Kaneda] (JP 2003-216506).

As per Claim 1, Kaneda discloses, "a rewritable nonvolatile memory" as **["semi-conductor flash memory" (Paragraph 0002)]** "and a control circuit" **["control circuit section " (Paragraph 0008)]** "wherein the memory apparatus brings logical addresses into correspondence with physical addresses of the nonvolatile memory and retains a piece of number-of-rewrites information for each logical address" **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table." (Paragraph 0008)]** "wherein the control circuit can perform a replacement process of a piece of memory information on the nonvolatile memory, and wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing data transfer according to the replacement" **["It is a thing possessing RAM in which the count table of writing which has memorized**

the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table. Moreover, a calculating machine rearranges OS field block to a free area by the read-out write request of the data area block from a host, writes said data area block in OS field block before rewriting and relocation, and is characterized by changing an address translation table" (Paragraph 0008 and 0009)].

As per Claim 2, Kaneda discloses "wherein the second physical address is a free physical address used for a correspondence with no logical address" as **["OS field block is rearranged to a free area by the read-out write request of a data area block" (Paragraph 0008)].**

As per Claim 3, Kaneda discloses "wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having the small number of rewrites," as **["At step 501, it writes in with reference to the count table of writing of the block in a flash memory, and a count is checked. With this check, it writes in at step 502 and existence of the block with many counts, existence of the block currently written in more than the count to which the count of writing was set, etc. are judged, and when there is no block with many counts**

of writing applicable to these, processing is ended. When there is a block with many counts of writing, it writes in at step 503, and the block with few [the minimum or] counts is selected," (Paragraph 0025)] "wherein the second logical address is changed so as to be brought into correspondence with the first physical address to which the given logical address having the small number of rewrites was assigned" **["and it writes in at step 504, and writes in with the block with many counts, and exchange processing with the block with few [the minimum or] counts is performed. Then, the block of an exchange place is copied to RAM206 at step 505, and a flag is set up to the block of a changing agency, and the block of an exchange place at step 506. Exchange processing of the block in a flash memory is carried out at step 507, an address translation table is rewritten at step 508, it changes at step 509, and a flag is cleared." (Paragraph 0025)].**

As per Claim 4, Kaneda discloses, "wherein the replacement process can be performed concurrently with a process in response to a direction for writing provided from an outside of a memory card" as **["Even if the 2nd object of this invention has access from a host at the time of the data exchange in a flash memory, it is to offer the storage and the computer which can replace a data area" (Paragraph 0007)]**

As per Claim 5, Kaneda discloses, "wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process

in response to the direction for writing reaches a given number of times" as **["and OS field before relocation is used as a data area, and the count of writing of the whole field of a flash memory is written in and it brings close to the count of a limitation, in this example, reinforcement is in drawing, using the whole flash memory effectively. In the condition 2, when the data of a data area (1) are read and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count," (Paragraph 0018 and 0019)].**

As per Claim 6, Kaneda discloses, "wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses" as **["In the condition 2, when the data of a data area (1) are read and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count, and it can bring close to the count of a write-in limitation. At this time, conversion of the logical address by having**

rearranged and a physical address is performed, and that result is memorized to an address translation table. Moreover, when it distinguishes whether the count which the count of writing of this block wrote in and was set up with reference to the count table is become when the data of a data area (1) are read and a write request occurs and the set-up count is become about it, you may make it rearrange. By doing in this way, the frequency of relocation decreases and a rewriting rate can be gathered. (Paragraph 0019 and 0020)].

As per Claim 7, Kaneda discloses, "wherein during the process in response to the direction for writing, the control circuit brings the logical address targeted for the process into correspondence with a third physical address and performs data rewrite" as **["the rewriting frequency of each rewriting block is measured, each sector of the block judged that rewriting frequency is high is moved to another specific block, namely, the management method move a logic storing block to the physical block of an expansion field is indicated by by carrying out counting of the count of elimination of the block which stored four sector data, and recording it." (Paragraph 0004)].**

As per Claim 8, Kaneda discloses, "wherein the nonvolatile memory has an address translation table in which correspondences of the logical addresses and physical addresses are defined" as **["The address translation table the control**

circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be," (Paragraph 0008)].

As per Claim 9, Kaneda discloses, "wherein the number-of-rewrites information for each logical address is retained in a region of the physical address corresponding to the logical address" **["Moreover, since RAM is volatile memory, if feed is no longer performed by the power off of a system, as for the management information in the translation table 207 of RAM206 of the control circuit section 202, the count table 208 of writing, and the exchange condition table 209, data will disappear. in order to avoid this -- the inside of the control circuit section 202 -- the power off judging change circuit 205 -- ****** from a system -- **** -- things are distinguished, the feed to the control circuit section 202 and a flash memory is changed to a dc-battery 203, and the data in RAM206 are evacuated to a flash memory." (Paragraph 0022) "the managed table of RAM206 in the control circuit section 202, and each condition of a condition 1 to the condition 3 is equivalent to each condition shown in drawing 3 . A managed table consists of an address translation table, data semantics, a count table of writing, and an exchange condition table." (Paragraph 0023)].**

As per Claim 10, Kaneda discloses, "wherein the number-of-rewrites information for each logical address is retained in a number-of-rewrites table" as **["It is a thing possessing RAM in which the count table of writing which has memorized the**

counts of writing for every block unit including OS field was prepared" (Paragraph 0008)].

As per Claim 11, Kaneda discloses, "a rewritable nonvolatile memory" as **["semi-conductor flash memory" (Paragraph 0002)]** "and a control circuit" **["control circuit section " (Paragraph 0008)]** "wherein the memory card brings logical addresses into correspondence with physical addresses of the nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address" **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table." (Paragraph 0008)]** "wherein the control circuit can executes are write process of the nonvolatile memory in response to a direction for writing from an outside, and a replacement process of memory information on the nonvolatile memory" **["writes said data area block in OS field block" (Paragraph 0009) It is inherent that the control block can write the memory.]** "wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites

information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing data transfer according to the replacement" **["It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table. Moreover, a calculating machine rearranges OS field block to a free area by the read-out write request of the data area block from a host, writes said data area block in OS field block before rewriting and relocation, and is characterized by changing an address translation table" (Paragraph 0008 and 0009)].**

As per Claim 12, Kaneda discloses, "A controller, performing host interface control and memory control on a rewritable nonvolatile memory" as **["semi-conductor flash memory" (Paragraph 0002) "control circuit section " (Paragraph 0008)]** "wherein the memory control includes control of bringing logical addresses into correspondence with physical addresses of the non volatile memory to manage a piece of number-of-rewrites information for each logical address" **["The address translation table the control circuit section has remembered conversion of the logical address and the physical address for every block unit of a flash memory to be, It is a thing possessing RAM in which the count table of writing which has**

memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table." (Paragraph 0008)] "and control of a replacement process that can be executed in performing rewrite on the nonvolatile memory, and wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the pieces of number-of-rewrites information with a second physical address so as to bring the given logical address into another correspondence with the second physical address and performing data transfer according to the replacement **["It is a thing possessing RAM in which the count table of writing which has memorized the counts of writing for every block unit including OS field was prepared. OS field block is rearranged to a free area by the read-out write request of a data area block, said data area block is written in OS field block before rewriting and relocation, and it is characterized by changing an address translation table. Moreover, a calculating machine rearranges OS field block to a free area by the read-out write request of the data area block from a host, writes said data area block in OS field block before rewriting and relocation, and is characterized by changing an address translation table" (Paragraph 0008 and 0009)].**

As per Claim 13, Kaneda discloses, "wherein the second physical address is a free physical address used for correspondence with no logical address" as **["OS field block is rearranged to a free area by the read-out write request of a data area block" (Paragraph 0008)].**

As per Claim 14, Kaneda discloses, "wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having the small number of rewrites," as **["At step 501, it writes in with reference to the count table of writing of the block in a flash memory, and a count is checked. With this check, it writes in at step 502 and existence of the block with many counts, existence of the block currently written in more than the count to which the count of writing was set, etc. are judged, and when there is no block with many counts of writing applicable to these, processing is ended. When there is a block with many counts of writing, it writes in at step 503, and the block with few [the minimum or] counts is selected," (Paragraph 0025)]** "wherein the second logical address is changed so as to be brought into correspondence with the first physical address to which the given logical address having the small number of rewrites was assigned" **["and it writes in at step 504, and writes in with the block with many counts, and exchange processing with the block with few [the minimum or] counts is performed. Then, the block of an exchange place is copied to RAM206 at step 505, and a flag is set up to the block of a changing agency, and the block**

of an exchange place at step 506. Exchange processing of the block in a flash memory is carried out at step 507, an address translation table is rewritten at step 508, it changes at step 509, and a flag is cleared." (Paragraph 0025)].

As per Claim 15, Kaneda discloses, "wherein the replacement process can be performed concurrently with a process in response to a direction for writing on a volatile memory provided from an outside thereof" as **["Even if the 2nd object of this invention has access from a host at the time of the data exchange in a flash memory, it is to offer the storage and the computer which can replace a data area" (Paragraph 0007)].**

As per Claim 16, Kaneda discloses, "wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process in response to the direction for writing reaches a given number of times" as **["and OS field before relocation is used as a data area, and the count of writing of the whole field of a flash memory is written in and it brings close to the count of a limitation, in this example, reinforcement is in drawing, using the whole flash memory effectively. In the condition 2, when the data of a data area (1) are read and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By**

repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count," (Paragraph 0018 and 0019)].

As per Claim 17, Kaneda discloses, "wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses" as **["In the condition 2, when the data of a data area (1) are read and a write request occurs, it replaces by relocating the data of OS field (1) to a free area, and data are written in by making OS field before relocation (1) into a data area (1). As a result of this relocation, as shown in a condition 3, the count of writing of a data area (1) and a free area is set to 2 and 10, respectively. By repeating this processing, near of the count of writing of the whole flash memory can be carried out to the same count, and it can bring close to the count of a write-in limitation. At this time, conversion of the logical address by having rearranged and a physical address is performed, and that result is memorized to an address translation table. Moreover, when it distinguishes whether the count which the count of writing of this block wrote in and was set up with reference to the count table is become when the data of a data area (1) are read and a write request occurs and the set-up count is become about it, you may make it rearrange. By doing in this way, the frequency of relocation decreases and a rewriting rate can be gathered. (Paragraph 0019 and 0020)].**

CLOSING COMMENTS

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

10. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

11. Per the instant office action, **Claims 1-17** have received a first action on the merits and are subject of a first action non-final.

12. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

13. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth M. Lo whose telephone number is 571-272-9774. The examiner can normally be reached on Mon - Thu (7:30am - 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sub (Sam) Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kenneth Lo
Art Unit: 2188

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
11/07/07